In the Claims:

1. (Currently Amended) A nonvolatile memory cell comprising:

having a vertical field-effect transistor with a nanoelement designed as the channel region, the nanoelement containing at least one of a nanotube, a bundle of nanotubes, or a nanorod; and

having an electrically insulating layer, which at least partially surrounds the nanoelement, as a charge storage layer and as a gate-insulating layer, which is designed in such a manner that electrical charge carriers can be selectively introduced into or removed from the electrically insulating layer and anit; the electrical conductivity of the nanoelement can be influenced in a characteristic way by electrical charge carriers introduced in the electrically insulating layer.

2. (Currently Amended) The memory cell as claimed in claim 1, wherein in which the electrically insulating layer is a silicon oxide/silicon nitride/silicon oxide layer sequence;, or an aluminum oxide layer.

3. (Cancelled)

4. (Currently Amended) The memory cell as claimed in claim 31, wherein in which the nanorod includes silicon, germanium, indium phosphide, gallium nitride, gallium arsenide, zirconium oxide, and/or a metal.

5. (Currently Amended) The memory cell as claimed in claim 31, wherein in which the nanotube is a carbon nanotube, a carbon-boron nanotube, a carbon-nitrogen nanotube, a tungsten sulfide nanotube, or a chalcogenide nanotube.

6. (Currently Amended) The memory cell as claimed in one of claims 1 to 5claim 1, which includesfurther comprising a first electrically conductive layer as a first source/drain region of the field-effect transistor, on which the nanoelement is grown.

7. (Currently Amended) The memory cell as claimed in claim 6, in whichwherein the first electrically conductive layer is made

~~from~~comprises a catalyst material for catalyzing the formation of the nanoelement.

8. (Currently Amended) The memory cell as claimed in ~~one of claims 1 to 7~~claim 1, ~~which includes~~further comprising a second electrically conductive layer as a gate region of the field-effect transistor, which at least partially surrounds the electrically insulating layer.

9. (Currently Amended) The memory cell as claimed in claim 8, wherein a ~~in which the~~ thickness of the second electrically conductive layer is less than a longitudinal extent of the nanoelement~~,~~ such that the electrically insulating layer which surrounds the nanoelement and the second electrically conductive layer form a ring structure surrounding part of the nanoelement.

10. (Currently Amended) The memory cell as claimed in ~~one of claims 1 to 9, which includes~~ claim 1, further comprising a third electrically conductive layer as second source/drain region of the field-effect transistor, ~~which~~ the third electrically conductive layer is formed on the nanoelement.

11. (Currently Amended) The memory cell as claimed in ~~one of claims 1 to 10~~claim 1, wherein the memory cell is formed at least one of on ~~and/~~or in a substrate made from polycrystalline or amorphous material.

12. (Currently Amended) The memory cell as claimed in ~~one of claims 1 to 11, which is~~claim 1, wherein the memory cell is formed exclusively from dielectric material, metallic material and ~~the~~ a material of the nanostructure.

13. (Currently Amended) A memory cell array having a plurality of memory cells as claimed in ~~one of claims 1 to 12~~claim 1 formed at least one of next to ~~and/~~or on top of one another.

14. (Currently Amended) A method for fabricating a nonvolatile memory cell, ~~in which~~the method comprising:

forming a vertical field-effect transistor ~~is formed~~ with a nanoelement designed as the channel region, the nanoelement containing at least one of a nanotube, a bundle of nanotubes, or a nanorod; and

forming an electrically insulating layer, which at least partially surrounds the nanoelement, ~~is formed~~ as a charge storage layer and as a gate-insulating layer~~;~~, wherein the electrically insulating layer is designed ~~in~~ such ~~a manner~~ that electrical charge carriers can be selectively introduced into or removed from ~~it; the~~ the electrically insulating layer and an electrical conductivity of the nanoelement can be influenced in a characteristic way by electrical charge carriers introduced in the electrically insulating layer.

15. (Currently Amended) The method as claimed in claim 14, ~~in which~~further comprising:

forming a first electrically conductive layer ~~is formed~~ as a first source/drain region of the field-effect transistor;

forming ~~then~~ a second electrically conductive layer ~~is formed~~ as a gate region of the field-effect transistor;

uncovering a subregion of the first electrically conductive layer ~~is uncovered~~ by a via hole being introduced into the second electrically conductive layer;

forming the electrically insulating layer ~~is formed~~ on ~~the~~ a surface of the via hole; and

growing the nanoelement ~~is grown~~ in the via hole on the uncovered subregion of the first electrically conductive layer.

16. (Currently Amended) The method as claimed in claim 14, ~~in which~~further comprising:

forming a first electrically conductive layer ~~is formed~~ as a first source/drain region of the field-effect transistor;

forming ~~then~~ an auxiliary layer ~~is formed~~;

uncovering a subregion of the first electrically conductive layer ~~is uncovered~~ by a via hole being introduced into the auxiliary layer;

growing the nanoelement ~~is grown~~ in the via hole on the uncovered subregion of the first electrically conductive layer;

the auxiliary layer is removed; and

applying the electrically insulating layer ~~is applied~~ to ~~the~~ a surface of the nanoelement.

17. (Currently Amended) The method as claimed in claim 14, ~~in which~~ initially growing the nanoelement ~~is initially grown~~ vertically while standing freely on a source/drain region, and then forming a ~~the~~ remainder of the vertical field-effect transistor ~~is formed~~.

18. (New) A nonvolatile memory cell comprising:

a substrate;

a first electrically conductive layer disposed on the substrate;

a channel region formed by a nanoelement disposed on the first electrically conductive layer extending vertically on the substrate, the nanoelement containing at least one of a nanotube, a bundle of nanotubes, or a nanorod;

a first electrically insulating layer at least partially surrounding the nanoelement;

a second electrically conductive layer at least partially surrounding the first electrically insulating layer; and

a third electrically conductive layer on the nanoelement.

19. (New) The memory cell as claimed in claim 18, wherein the first electrically conductive layer comprises a catalyst material for catalyzing formation of the nanoelement.

20. (New) The memory cell as claimed in claim 18, wherein a thickness of the second electrically conductive layer is less than a longitudinal extent of the nanoelement such that the first electrically insulating layer which surrounds the nanoelement and the second electrically conductive layer form a ring structure surrounding part of the nanoelement.

21. (New) The memory cell as claimed in claim 18, further comprising electrically insulating decoupling elements disposed between the second and third electrically conductive layers.

22. (New) The memory cell as claimed in claim 18, wherein the first electrically insulating layer is disposed between the second and third electrically conductive layers.

23. (New) The memory cell as claimed in claim 18, further comprising a second electrically insulating layer at least partially surrounding the second electrically conductive layer.

24. (New) The memory cell as claimed in claim 23, wherein the nanoelement is planar with the second electrically insulating layer.

25. (New) The memory cell as claimed in claim 23, wherein the nanoelement is non-planar with the second electrically insulating layer such that the nanoelement extends farther from the substrate than the second electrically insulating layer.

26. (New) The memory cell as claimed in claim 23, wherein the second electrically conductive layer contacts an end of the nanoelement and an upper surface of the second electrically insulating layer.

27. (New) The memory cell as claimed in claim 18, further comprising a third electrically insulating layer disposed between the first and second electrically conductive layers.